REMARKS

Claims 1-35 are pending in the application. Please amend Claims 4, 13, 23, 25, and 27. Applicants respectfully request entry of the foregoing amendments to Claims 4, 13, 23, 25, and 27 prior to further examination. No new matter has been introduced.

Regarding Claim Amendments

Claims 4 and 13 have been amended to include a colon after the word "comprises". Claims 23 and 25 have been amended to correct for typographical errors. No new matter has been introduced.

Regarding Section 112 Rejections

Claims 27-31 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner indicated the view that "the particular subsystem" as referenced in Claims 27-30 lacks clear antecedent basis.

Applicants have amended "the particular subsystem" of Claim 27 to read "a particular subsystem". As such, amended Claim 27 has clear antecedent basis. Applicant respectfully requests the withdrawal of the rejection of Claim 27 under 35 U.S.C. 112.

Claims 28-31 depend from amended Claim 27 and now have clear antecedent basis. Applicant respectfully requests the withdrawal of the rejection of Claims 28-31 under 35 U.S.C. 112.

Regarding Section 103 Rejections

Claims 1-3, 10-12, 16, and 21-22 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Brown (U.S. Patent No. 6,185,520) in view of well known features, as evidenced by Geusic (U.S. Patent Application No. 20010026439). The rejection is respectfully traversed.

The present invention relates to a "system on a chip" including multiple subsystems 102 interconnected through an on-chip bus 104. Each subsystem 102 includes core logic and a

respective data transfer unit 108 for facilitating communication between corresponding subsystems 102 on the "system on a chip" via the on-chip bus 104. Each data transfer unit 108 includes a number of pairs of outbound and inbound transaction queues 402 and 404, an outbound transaction queue state machine 406, and an inbound transaction queue state machine 408. (*See* Specification, page 4, line 5 through page 5, line 15; page 11, lines 2-16; and FIGS. 1 and 4-6).

The outbound transaction queue service state machine 406 processes the transactions placed into the outbound queues 402 in order of the assigned priorities of the outbound queue 402 and the inbound queue 404. For each of the transactions being serviced, the outbound transaction queue service state machine 406 provides the control signals to the corresponding outbound queue 402 to output on the subsystem's request lines, the included bus arbitration priority of the first header of the "oldest" (in turns of time queued) transaction of the queue 402, to arbitrate and compete for access to bus 104 with other contending transactions of other subsystems 102. Upon being granted access to bus 104, the outbound transaction queue service state machine 406 provides the control signals to the outbound queue 402 to output the remainder of the transaction. (*See* Specification, page 11, line 16 through page 12, line 11; and FIGS. 1 and 4-6).

Similarly, the inbound transaction queue service state machine 408 provides the control signals to the corresponding inbound queue 404 to claim a transaction on bus 104, if it is determined that the transaction is a new request transaction of the subsystem 102 or a reply transaction to an earlier request transaction of the subsystem 102. Additionally, if the claiming of a transaction changes the state of the inbound queue 404 from empty to non-empty, the inbound transaction queue service state machine 408 also asserts a "non-empty" signal for the core logic of the subsystem 102. (*See* Specification, page 12, lines 12-19; and FIGS. 1 and 4-6).

Brown provides a computer system 500 including a switch 201 having a plurality of ports 222-225, each port 222-225 adapted to be coupled to a respective one of a plurality of peripheral devices. Each ports 222-225 is further adapted to accept data from its respective device and transmit data to its respective device in a bi-directional manner. The switch 201 couples a first pair of the plurality of ports to enable communication between their respective devices and couples a second pair of the plurality of ports to enable communication between their respective

devices such that communication between the first pair of ports and communication between the second pair of ports occurs simultaneously and independently, thereby implementing efficient switched data transfers between the respective devices and greatly increasing the total data transfer bandwidth of the computer system. The switch is not "a system on a chip", it does not include on-chip subsystems, and it does not include an on-chip bus, rather the switch is simply a "switch" that interconnects peripheral devices.

The switch 201 includes multiple input queues 610-612 respectively coupled to port 222, port 223, and port 224. Each of input queues 610-612 is coupled to output queues 631, 632. The input queues 610-612 implement the "store and forward" functionality of switch 201 and the output queues 631-632 implement the prioritization functionality of switch 201, wherein higher priority data is forwarded before lower priority data. There is no disclosure in Brown that would indicate the input queues include an input state machine or the output queues include an output state machine.

Geusic provides an electronic assembly including a semiconductor interposer having first and second surfaces. The semiconductor interposer also has cooling channels passing through the interposer between the first and second surfaces. The electronic assembly has at least one semiconductor chip disposed outwardly from the first surface of the semiconductor interposer and at least one semiconductor chip disposed outwardly from the second surface of the semiconductor interposer. The electronic assembly also has a number of electrical connections through the semiconductor interposer wherein the number of electrical connections couple the semiconductor chips disposed outwardly from the first and second surfaces of the semiconductor interposer. The number of electrical connections teaches away from a common on-chip bus. Further, Geusic suggests that there is a growing desire for a "system on a chip" but in practice it is very difficult to implement a "system on a chip." As a compromise, "chip-on-chip" systems have been developed. These "chip-on-chip" systems also do not utilize an on-chip bus, rather they interconnect via numerous electrical connections.

Neither Brown nor Geusic, alone or in combination, teach, suggest, or otherwise make obvious "a first and a second outbound queue to facilitate selective staging of a first and a second plurality of outbound bus transactions for the on-chip subsystem, at the choosing of the on-chip subsystem, each of said outbound bus transactions including a bus arbitration priority and a first

state machine coupled to the first and second outbound queues to service the first and second outbound queues by according the first queue a first outbound priority and the second queue a second outbound priority, and serially requesting for access to the on chip bus for the staged outbound bus transactions based at least in part on accorded outbound priorities, where access to the on-chip bus is granted to requesting bus transactions based at least in part on the included bus arbitration priorities of the contending bus transactions" because Brown teaches a "switch" for connecting peripheral devices and a "switch" is not a "system on a chip" including on-chip subsystems, an on-chip bus, or a first state machine as claimed in Claim 1 of the present invention. Further, Geusic specifically states "is very difficult to implement a 'system on a chip'" and chip-to-chip designs have been used as a compromise. Thus, the prior art does not teach or suggest a "system on a chip" including an on-chip bus as claimed in Claim 1. Furthermore, Claim 1 recites that the first state machine serially requests access to the on-chip bus based at least in part on outbound priorities, while access to the bus is granted based at least in part on bus arbitration priorities. It is clear from this language that there exists two different types of priorities, e.g., a bus arbitration priority and an outbound priority. Neither Brown nor Geusic teach or suggest two different types of priorities, e.g., a bus arbitration priority and an outbound priority as claimed in Claim 1. Claim 10 includes similar limitations as Claim 1 and is allowable for the same reasons. As such, Applicant respectfully requests the withdrawal of the rejection of Claims 1 and 10 under 35 U.S.C. 103.

Claims 2 and 3 depend from Claim 1 and Claims 11, 12, and 16 depend from Claim 10 and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of Claims 2, 3, 11, 12, and 16 under 35 U.S.C. 103.

With respect to Claim 21, neither Brown nor Geusic, alone or in combination, teach, suggest, or otherwise make obvious "determining intra-subsystem priorities for transactions with others subsystems of the integrated circuit to be serviced for requesting access to an on-chip bus of the integrated circuit, to which the subsystems are coupled; generating and staging the transactions in accordance with the determined intra-subsystem priorities, including with each of the staged transactions a bus arbitration priority for use to arbitrate for access to the on-chip bus with other inter-subsystem transactions of other subsystems of the integrated circuit; and serially servicing the staged transactions in accordance with their intra-subsystem priorities, requesting

access to the on-chip bus for each staged transaction being serviced using the included bus arbitration priority" as claimed in Claim 21 because Brown teaches a "switch" for connecting peripheral devices and a "switch" is not a "system on a chip" including on-chip subsystems or an on-chip bus. Further, Geusic specifically states "is very difficult to implement a 'system on a chip'" and chip-to-chip designs have been used as a compromise. Thus, the prior art does not teach or suggest a "system on a chip" including accessing an on-chip bus as claimed in Claim 21. Furthermore, as stated above, neither Brown nor Geusic teach or suggest two different types of priorities, e.g., a bus arbitration priority and an outbound priority as claimed in Claim 21. As such, Applicant respectfully requests the withdrawal of the rejection of Claim 21 under 35 U.S.C. 103. Claim 22 depends from Claim 21 and is allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of Claim 22 under 35 U.S.C. 103.

Claims 4-6 and 13-15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Brown in view of Bergeson (U.S. Patent No. 6784890). Claims 4-6 depend from Claim 1 and Claims 13-15 depend from Claim 10 and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of Claims 4-6 and 13-15 under 35 U.S.C. 103.

Claims 7-9, 17-20, and 23-35 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Brown in view of Bergeson, and further in view of well known features, as evidenced by Geusic. The rejection is respectfully traversed.

Bergeson discloses a method for controlling expedite cycles having the steps of determining the number of clock cycles devoted to expedite data transfer requests made to a component during a predetermined monitoring window and guaranteeing a minimum number of clock cycles processing non-expedite requests during the monitoring window. There is no disclosure in Bergeson that would indicate a state machine serially bring staged transactions to the attention of a subsystem based at least in part on the inbound priorities it has accorded to the inbound queues. Further, is no disclosure in Bergeson that would indicate there are at least two different types of priorities for managing traffic on the on-chip bus.

Further, Bergeson does not teach, suggest, or otherwise make obvious a state machine serially bring staged transactions to the attention of a subsystem based at least in part on the inbound priorities it has accorded to the inbound queues or at least two different types of

priorities for managing traffic on the on-chip bus. Claims 8-9 depend from Claim 7 and Claims 18-20 depend from Claim 17 and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of Claims 7-9 and 17-20 under 35 U.S.C. 103.

As stated above, Brown, alone or in combination, does not teach, suggest, or otherwise make obvious the limitations of independent Claim 21. Claims 23 and 24 depend from Claim 21 and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of Claims 23 and 24 under 35 U.S.C. 103.

Neither Brown, Bergeson, nor Geusic, alone or in combination, teach, suggest, or otherwise make obvious "staging transactions from other subsystems in a priority based manner as requested by originating subsystems of the transactions, each of said transactions from other subsystems having a bus arbitration priority, on which access to an on-chip bus the subsystems are coupled was granted; and serially servicing the staged transactions from other subsystems, notifying core logic of the subsystem, in accordance with the priority based manner the transactions from other subsystems are staged" as claimed in Claim 21 because Brown teaches a "switch" for connecting peripheral devices and a "switch" is not a "system on a chip" including subsystems, subsystems coupled to an on-chip bus, or notifying core logic of each subsystem. Further, Geusic specifically states "is very difficult to implement a 'system on a chip'" and chip-to-chip designs have been used as a compromise. Thus, the prior art does not teach or suggest a "system on a chip" including an on-chip bus as claimed in Claim 21. Claim 26 depends from Claim 25 and is allowable for the same reasons. As such, Applicant respectfully requests the withdrawal of the rejection of Claims 25 and 26 under 35 U.S.C. 103.

Neither Brown, Bergeson, nor Geusic, alone or in combination, teach, suggest, or otherwise make obvious "an on-chip bus; and a plurality of subsystems coupled to the on-chip bus and interact with each other through transactions conducted across said on-chip bus, with each of the subsystems having a data transfer interface that interfaces the subsystem to the on-chip bus, and at least one of the data transfer interfaces allows a particular subsystem to initiate transactions with other subsystems in a prioritized manner, including a first intra-subsystem prioritization on the order transactions contending for the service of the at least one of the data transfer interfaces are to be serviced, and a second inter-subsystem prioritization on the order transactions of the various subsystems contending for the on-chip bus are to be granted access to

the on-chip bus" as claimed in Claim 27 because Brown teaches a "switch" for connecting peripheral devices and a "switch" is not a "system on a chip" including an on-chip bus, a plurality of subsystems coupled to the on-chip bus, and each of the subsystems having a data transfer interface that interfaces the subsystem to the on-chip bus. Further, Geusic specifically states "is very difficult to implement a 'system on a chip'" and chip-to-chip designs have been used as a compromise. Thus, the prior art does not teach or suggest a "system on a chip" including an on-chip bus as claimed in Claim 27. Claims 28-31 depend from Claim 27 and are allowable for the same reasons. As such, Applicant respectfully requests the withdrawal of the rejection of Claims 27-31 under 35 U.S.C. 103.

Neither Brown, Bergeson, nor Geusic, alone or in combination, teach, suggest, or otherwise make obvious "a first subsystem having a first data transfer interface interfacing the first subsystem to the on-chip bus, initiating first transactions with other subsystems through selective employment of facilities of the first data transfer interface to internally prioritizing the order the first transactions are to be serviced by the first data transfer interface, and including with said first transactions first bus arbitration priorities to facilitate prioritization of granting of access to the on-chip bus to contending inter-subsystem transactions including said first transactions; and a second subsystem having a second data transfer interface interfacing the second subsystem to the on-chip bus, initiating second transactions with other subsystems through selective employment of facilities of the second data transfer interface to internally prioritizing the order the second transactions are to be serviced by the second data transfer interface, and including with said second transactions second bus arbitration priorities to facilitate prioritization of granting of access to the on-chip bus to contending inter-subsystem transactions including the second transactions" as claimed in Claim 32 because Brown teaches a "switch" for connecting peripheral devices and a "switch" is not a "system on a chip" including an on-chip bus, a first subsystem having a first data transfer interface interfacing the first subsystem to the on-chip bus and second subsystem having a second data transfer interface interfacing the second subsystem to the on-chip bus. Further, Geusic specifically states "is very difficult to implement a 'system on a chip'" and chip-to-chip designs have been used as a compromise. Thus, the prior art does not teach or suggest a "system on a chip" including an on-chip bus as claimed in Claim 32. Claims 33-35 depend from Claim 32 and are allowable for the
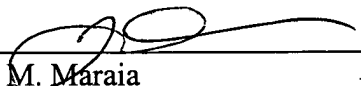
same reasons. As such, Applicant respectfully requests the withdrawal of the rejection of Claims 32-35 under 35 U.S.C. 103.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims (1-35) are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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